B. Chitti Gowri* et al.
(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH
Volume No.4, Issue No.1, December - January 2016, 2569 – 2576.

Enhancement of Voltage Sag & Transient Stability Using Resistive Type SFCL for Fault Appearances

B.CHITTI GOWRI
M.Tech Student Scholar (P.E)
Department of Electrical and Electronics Engineering,
KITS College of Engineering, Divili
(Affiliated to JNTU Kakinada), A.P, India

K. ARUN KUMAR
Assistant Professor, M.Tech.,
Department of Electrical and Electronics Engineering,
KITS College of Engineering, Divili
(Affiliated to JNTU Kakinada), A.P, India

Abstract- **The proposed structure prevents voltage sag and phase-angle jump of the substation PCC after fault occurrence. This paper proposes a new SFCL structure with a comparison of parallel-*LC*-resonance type fault current limiter (FCL) that uses a resistor in series with a capacitor to mitigate the faults in a distribution line. The proposed SFCL is capable of limiting the fault current magnitude near to the pre-fault magnitude of distribution feeder current by placing the mentioned resistor in the structure of the FCL. Several solutions have been implemented, including the use of Superconducting Fault Current Limiter (SFCL), in order to reduce circuit breakers rated capacity and to limit the electromagnetic stress in associated equipment. At first, a resistive type SFCL is modelled in Simulink. A three phase system with a regular capacity is designed and then it is replaced by higher capacity keeping switchgear unchanged. Finally, the SFCL is introduced in the higher capacity system. Thus, it is revealed that the outstanding current limiting performance of SFCL can be used to limit the fault to the level of the existing switchgear if the system capacity is improved. In order to evaluate the impact of fault current limiter in power system performance, simulation models of several compensation schemes are implemented with the help of Matlab/Simulink tool.**

Keywords: **Parallel-Resonance type Fault current limiter (FCL), point of common coupling (PCC), power quality (PQ), semiconductor switch, total harmonic distortion (THD), voltage sag.**

I. INTRODUCTION

Conventional protection devices installed for protection of excessive fault current in power systems, mostly at the high voltage substation level circuit breakers tripped by over-current protection relay which has a response-time delay resulting in power system to pass initial peaks of fault current [1]-[3]. It may result in decreasing the stability and reliability of the system. This huge short circuit current of higher capacity system is limited by fault current limiters which can be an alternative solution rather than replacing existing switchgear. High fault current can be limited to a level of highest designed short circuit current rating of presented switchgear. It creates a cost-effective way to improve the power system capacity keeping switchgear unchanged. Thus, the fault current limiter can be an excellent technique to protect power system equipments.

Voltage sag is an important PQ problem because of sensitive loads growth. Worldwide experience has show that short-circuit faults are the main origin of voltage sags and, therefore, there is a loss of voltage quality. This problem appears especially in buses which are connected to radial feeders [4]–[7]. Faults at either the transmission or distribution level may cause transient voltage sag or swell in the entire system or a large part of it. Also, under heavy load conditions, a significant voltage drop may occur in the system. Voltage sags can occur at any instant of time, with amplitudes ranging from 10–90% and a duration lasting for half a cycle to one minute. Further, they could be either balanced or unbalanced, depending on the type of fault and they could have unpredictable magnitudes, depending on factors such as distance from the fault and the transformer connections. Voltage swell, on the other hand, is defined as a sudden increasing of supply voltage up 110% to 180% in RMS voltage at the network fundamental frequency with duration from 10 ms to 1 minute.

But, SFCL is a novel technology which has the capability to quench fault currents instantly as soon as fault current exceeds SFCL's current limiting threshold level [8].

The traditional devices, used for fault current limitation, are:

1. Fuses are simple, reliable and they are usually used in low voltage and in middle voltage distribution grids. The main disadvantages are the single-use and the manually replacement of the fuses;
2. Circuit-breakers are commonly used, reliable protective devices. The circuit-breakers for high current interrupting capabilities are expensive and have huge dimensions. They require periodical

maintenance and have limited number of operation cycles;

3. Air-core reactor and transformers with increased leakage reactance increase the impedance of distribution network and consequently limit the short-circuit currents;

4. System reconfiguration and bus-splitting.

There have been an increase in the number of studies on the alternative solution to improve the reliability of electrical systems and one of them is the application of a fault current limiter (FCL). Many types of fault current limiter have been developed in the past few years [9]. Superconducting fault current limiter (SFCL) is the most inventive fault current limiting device [4]. It offers many advantages which include having no impact on the system in typical conditions, limiting fault current quickly and response automatically in an abnormal condition. In power system, studies of SFCL are anticipated not only to limit fault current but also to develop stability of the system [5-6]. Many studies have been carried out for the practical application of SFCL in electric power system in the past few years [10]-[14]. It includes current limiting characteristics of SFCL, optimal resistive value of SFCL to improve transient stability, optimal place to install the SFCL etc. But most of the important practical application concern of SFCL in power system to enhance system capacity with existing switchgear has not been studied.

In this paper, a resistive SFCL model is developed with the help of Simulink. The model is used in a three phase system to prove the current limiting behavior of the SFCL with a nominal capacity and the fault current characteristics are investigated.

II. FORMAL POWER CIRCUIT TOPOLOGY AND PRINCIPLES OF OPERATION

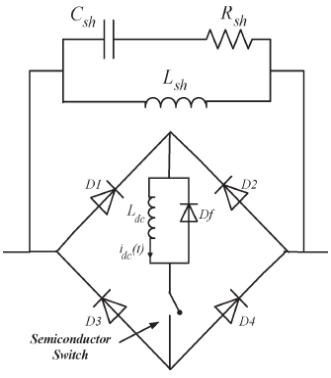


Fig. 1. Single-phase power circuit topology of the proposed parallel resonance- type FCL.

Fig. 1 shows the single-phase power circuit topology of the proposed FCL. It is necessary to use a similar circuit for each phase in a three-phase distribution system. This structure is composed of two main parts which are as follows.

1) Bridge part: This part consists of a rectifier bridge containing *D*1–*D*4 diodes, a small dc-limiting reactor (*L*dc), a self-turnoff semiconductor switch (such as a gate turnoff thyristor and an insulated-gate bipolar transistor) and its snubber circuit, and a freewheeling diode (*Df*).

2) Resonance part: This part consists of a parallel *LC* resonance circuit (*L*sh and *C*sh) (its resonant frequency is equal to power system frequency) and a resistor *R*sh in series with the capacitor. The bridge part of the proposed FCL operates as a high-speed switch that changes the fault current path to the resonance part when the fault occurs. Obviously, it is possible to substitute this part with an antiparallel connection of two self-turnoff semiconductor switches. The main disadvantage is while using the semiconductor switch needs a suitable snubber circuit for its protection, which is not shown in Fig. 2 for simplicity. Also, high-rating semiconductor switches, their protection procedure, and minimization of their power losses. From the power loss point of view, in the normal condition, the proposed FCL has the losses on the rectifier bridge diodes, the semiconductor switch, and the small resistance of the dc reactor. Each diode of the rectifier bridge is ON in half a cycle, while the semiconductor switch is always ON. Therefore, the power losses of this FCL in the normal operation is high & that may decreases the overall efficiency of the system can be calculated as

$$P_{\text{loss}} = P_R + P_D + P_{\text{SW}} = R_{\text{dc}} I_{\text{dc}}^2 + 4V_{\text{DF}} I_{\text{ave.}} + V_{\text{SWF}} I_{\text{dc}}$$

Where
*I*dc dc-side current which is equal to the peak of the line current (*I*peak);
*R*dc resistance of the dc reactor;
*V*DF forward voltage drops on each diode;
*V*SWF forward voltage drop on the semiconductor switch;
*I*ave. average current of the diodes in each cycle that is equal to *I*peak/*π*.

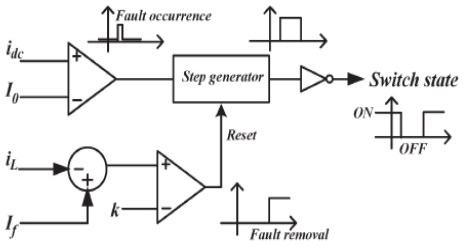


Fig. 2. Control circuit of the proposed FCL.

Fig. 2 shows the control circuit of the proposed FCL. In the normal operation of the power system, the semiconductor switch is ON. Therefore, *L*dc is

charged to the peak of the line current and behaves as a short circuit. Using the semiconductor devices (the diodes and semiconductor switch) and the small dc reactor causes a negligible voltage drop on the FCL. When a fault occurs, the dc current becomes greater than the maximum permissible current *I*0, and the control circuit detects it and turns the semiconductor switch off. Therefore, the bridge retreats from utility. At this moment, the freewheeling diode *Df* turns on and provides free path for discharging the dc reactor. When the bridge turns off, the fault current passes through the parallel resonance part of the FCL. Consequently, large impedance enters to the circuit and prevents the fault current from rising. In the fault condition, the parallel *LC* circuit starts to resonate. In this case, because of resonance, the line current oscillates with large magnitude. These oscillations may lead to damaging system equipment or putting them in stress. However, by placing a resistor (*R*sh) in series with the capacitor, current transients damp quickly. In addition, by using *R*sh, the voltage drop on *R*sh causes that the voltage across the capacitor is decreased during fault.

When the fault disappeared, while the semiconductor switch is OFF, the parallel part of the FCL will be connected in series with the load impedance. Therefore, the line current will be decreased instantaneously. To detect this instantaneous reduction of the line current, *iL* is compared with *If* that can be calculated from

$$I_f = \frac{|\overline{V}_{\mathrm{PCC}}|}{|Z_{\mathrm{eq}}|}$$

Where *Z*eq is the equivalent impedance of the resonance part. When the difference of *iL* and *If* becomes greater than *k* as the fault removal sign, the control circuit turns the semiconductor switch on. Therefore, the power system returns to the normal state. The value of *k* can be calculated from

$$k = \frac{|\overline{V}_{\mathrm{PCC}}|}{|\overline{Z}_{\mathrm{eq}}|} - \frac{|\overline{V}_{\mathrm{PCC}}|}{|\overline{Z}_{\mathrm{eq}} + \overline{Z}_{L,\min}|}$$

Where *ZL* ,min is the minimum impedance of the load on the protected feeder. As pointed, some of previously proposed FCL structures have ac power losses at the resonant circuit in the normal condition, because of placing a large inductor in the line current path. However, the proposed structure in this paper has very low losses in the normal condition, because the inductor is bypassed by the bridge part. Also, by choosing proper values for the resonant circuit, the proposed FCL limits the fault current in a way that the power system is not affected by the fault. In such condition, there will not be any considerable voltage sag on the PCC voltage.

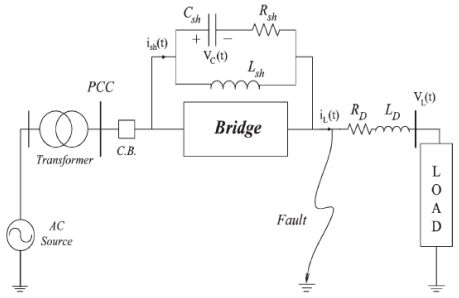


Fig. 3. Single-line diagram of the power system.

III. PROPOSED SUPER-CONDUCTING FCL

Superconducting fault current limiter is a promising technique to limit fault current in power system. Normally non-linear characteristic of superconductor is used in SFCL to limit fault current. In a normal operating condition SFCL has no influence on the system due to the virtually zero resistance below its critical current in superconductors. But when system goes to abnormal condition due to the occurrence of a fault, current exceeds the critical value of superconductors resulting in the SFCL to go resistive state. This capability of SFCL to go off a finite resistive value state from zero resistance can be used to limit fault current. Different types of SFCLs have been developed until now [15]-[25]. Many models for SFCL have been designed as resistor-type, reactor-type, and transformer-type etc. In this paper a resistive-type SFCL is modeled using simulink. Quench and recovery characteristics are designed on the basis of [26].

An impedance of SFCL according to time t is expressed by

$$R_{SFCL} = \begin{cases} 0, & (t_0 > t) \\ R_m\left[1 - \exp\left(-\frac{t - t_0}{T_{sc}}\right)\right]^{\frac{1}{2}}, & (t_0 \le t < t_1) \\ a_1(t - t_1) + b_1, & (t_1 \le t < t_2) \\ a_2(t - t_2) + b_2, & (t_2 \le t) \end{cases}$$

Where Rm is the maximum resistance of the SFCL in the quenching state, Tsc is the time constant of the SFCL during transition from the superconducting state to the normal state. Furthermore, t0 is the time to start the quenching. The working principle of the SFCL model developed in Simulink/Sim Power system is described below. Firstly, RMS value of incoming current (passing through current measurement block) is measured by RMS block. Then it compares the current with the specified current in the SFCL subsystem. SFCL gives

minimum resistance, if the incoming current is less than the triggering current level. But if the current is larger than the triggering current, SFCL's impedance rises to maximum state. It ultimately raises the total impedance of the system which results in limiting the fault current. Finally, the SFCL's resistance will be minimum when the limited fault current is below the triggering value.

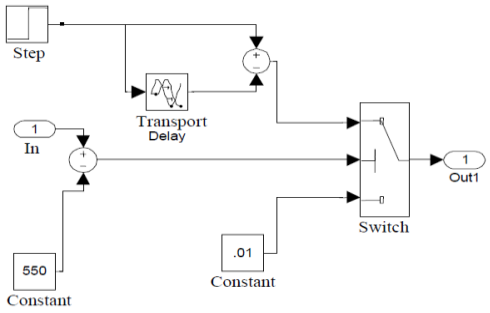


Fig.4 Implementation of Resistive SFCL Characteristics in Simulink

These parameters are used for implementing resistive SFCL characteristic is shown in Fig. 4. Quenching and recovery time of SFCL are specified using step and transport block respectively. A Switch block is used to give minimum or maximum impedance in output which is determined considering the incoming current. The simulation model of SFCL for a single phase system is shown in Fig. 3. Simulink/Sim Power system is chose to design resistive SFCL. Four fundamental parameters is used for modeling resistive-type SFCL [27]-[33]. The parameters and their values are: Transition or response time = 2ms, minimum impedance= 0.01Ω & maximum impedance= 20Ω, triggering current =550A, recovery time =10ms.

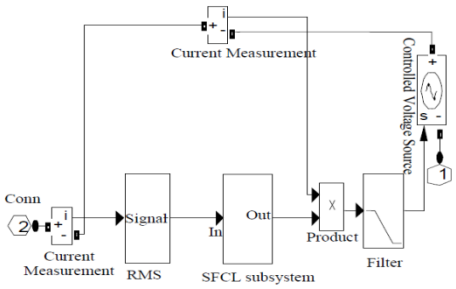


Fig.5 Resistive SFCL model in Simulink

The designed model of SFCL is implemented in single phase system and fault current characteristics are taken with and without SFCL. The fault is introduced directly through AC source in order to decrease the difficulty of simulation. An RMS block is used to calculate the RMS value of the incoming current and scope is used to see the output o the system.

IV. SIMULATION RESULTS

Case 1: *Three Phase Network without FCL.*

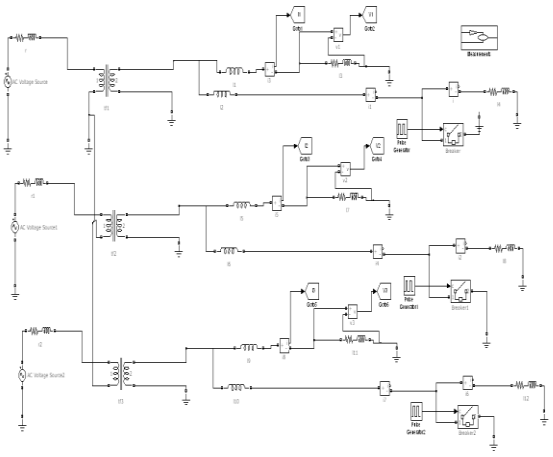


Fig 6. Matlab/Simulink circuit of PCC without FCL

Fig 6. Shows the Matlab/Simulink circuit of PCC without FCL using Matlab/Simulink Software Package.

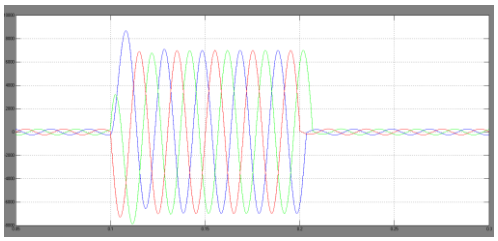


Fig.7 Three Phase Line Currents without FCL

Fig.7 shows the Three Phase Line Currents without FCL, due to sudden fault condition current goes to increases, limiting this current by using FCL.

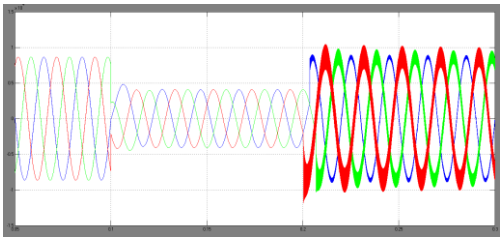


Fig.8 Three Phase Line Voltages without FCL

Fig.8 shows the Three Phase Line Voltages without FCL, due to sudden fault condition voltage may goes to decreases; maintain this voltage as constant by using FCL.

Case 2: Three Phase Network with FCL

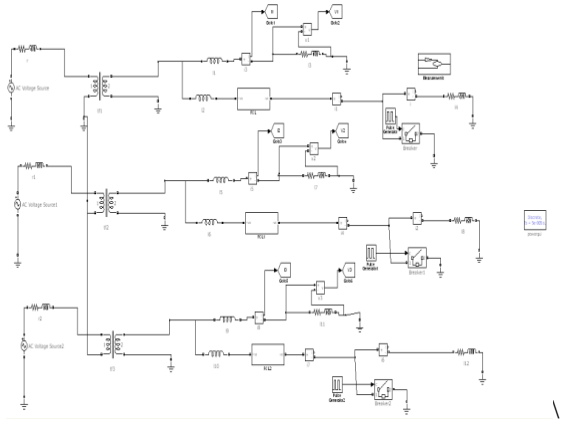


Fig 9. Matlab/Simulink circuit of PCC with FCL

Fig 9. Shows the Matlab/Simulink circuit of PCC with FCL using Matlab/Simulink Software Package.

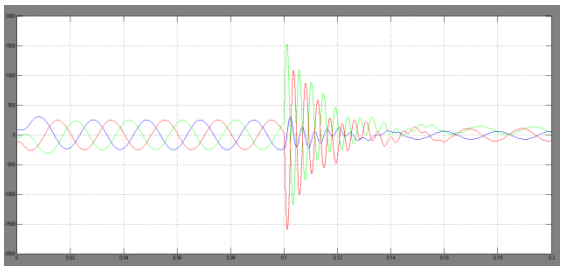


Fig.10 Three Phase Line Currents with FCL with No Rsh

Fig.10 shows the Three Phase Line Currents with FCL with No Rsh; due to that condition current value goes to increases & oscillated, limiting this current by using FCL with parallel resonance condition.

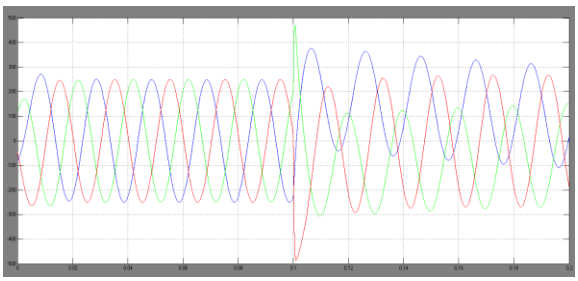


Fig.11 Three Phase Line Currents with Proposed FCL

Fig.11 shows the Three Phase Line Currents with Proposed FCL; due to this proposed FCL current value goes to limiting & less oscillated, limiting these oscillations in current by using FCL with parallel resonance condition.

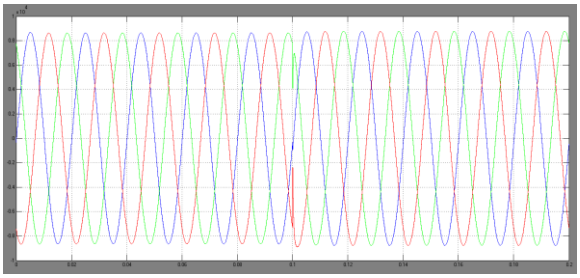


Fig. 12 Three phase PCC voltage with the proposed FCL.

Fig. 12 show the three phase voltage at PCC with the FCL. It is found to be undistorted voltage waveform even a fault has occurred.

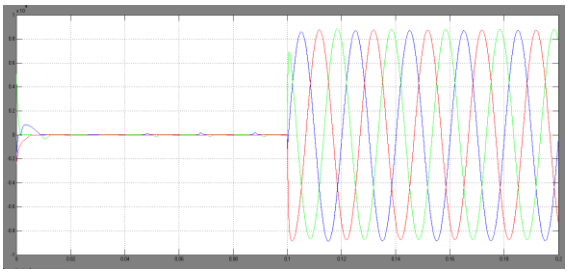
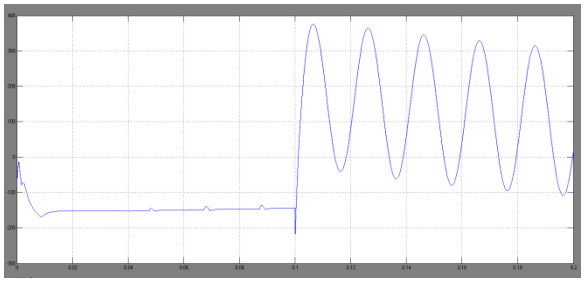
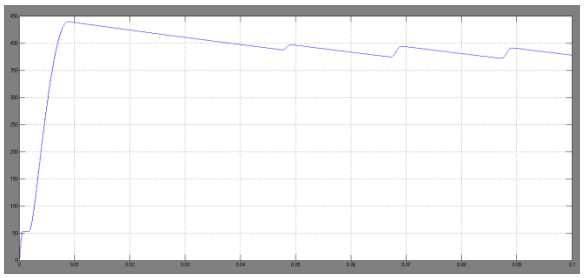


Fig. 13 Three phase Voltage drop on the proposed FCL during fault.

Fig. 13 shows the three phase voltage drop on the FCL during the fault. This voltage drop does not allow the PCC voltage to change.



(a)



(b)

Fig. 14 (a) Line, dc reactor, and (b) shunt impedance currents.

Fig. 14 shows the shunt impedance current for the three phase system.

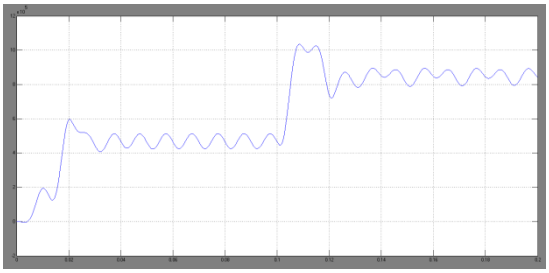


Fig.15 Total Power

Fig.15 shows the Total Power with Proposed FCL

Case 3: Three Phase Network with SFCL

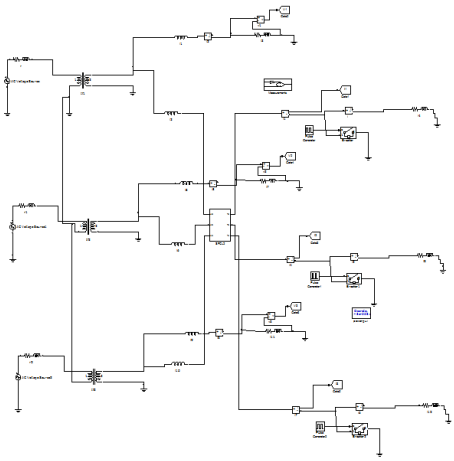


Fig 16. MATLAB/Simulink of the proposed SFCL circuit

Fig. 16 shows the MATLAB/Simulink model of the proposed SFCL circuit with fault condition.

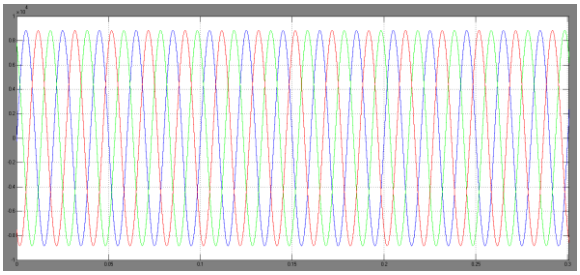


Fig. 17 Three phase PCC voltage with the proposed SFCL.

Fig. 17 show the three phase voltage at PCC with the SFCL. It is found to be undistorted voltage waveform compared to FCL, SFCL operation is so better to minimize the steady state error & maintain good stability factor.

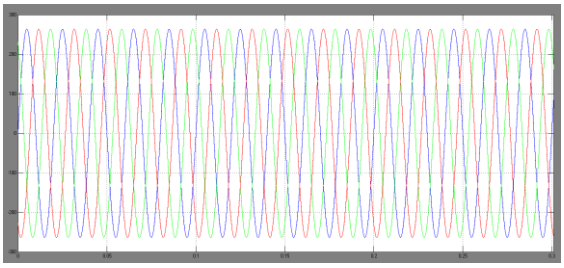


Fig.18 Three Phase Line Currents with Proposed SFCL

Fig.18 shows the Three Phase Line Currents with Proposed SFCL; due to this proposed SFCL current value goes to limiting & no oscillated, limiting these oscillations in current by using SFCL compared to parallel resonance FCL condition.

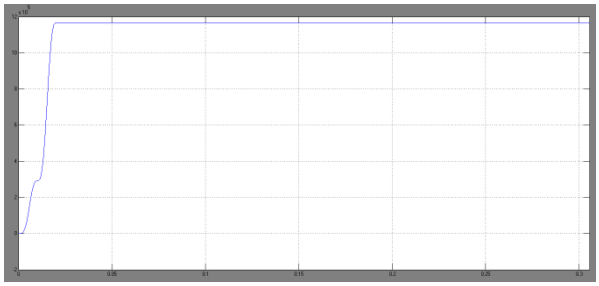


Fig. 19 Three-phase instantaneous power of the sensitive load with the proposed SFCL during fault condition

Fig. 19 shows the three-phase instantaneous power of the sensitive load with the proposed SFCL. It is seen that the power is remains unaltered during the fault condition.

V. CONCLUSION

The development of effective SFCLs is becoming very important in relation to rising fault current levels in modern power networks. The benefit of SFCLs application in power systems is reduction the current stresses on equipment during faults, transient stability of the power grid enhancement and reduction of voltage dips and sags. In this paper, a new topology of SFCL & parallel-*LC*-resonance-type FCL that includes a series resistor with the capacitor of the *LC* circuit has been introduced. The analytical analysis and design considerations for both structures have been presented. The overall operation of the mentioned SFCL in normal and fault conditions has been studied in detail. Also, the simulation results have been involved to validate the analytic analyses. All proposed SFCLs have good current-limiting characteristics compared to FCL operation & maintain good stability factor with more reliable operation. In addition to that the SFCL is developed for the three phase power system &, SFCL maintain constant voltage at my PCC their behaviors with and without the FCL are observed using Simulink results.

VI. REFERENCES

[1] M. Jafari, S. B. Naderi, M. Tarafdar Hagh, M. Abapour, and S. H. Hosseini, "Voltage sag compensation of point of common coupling (PCC) using fault current limiter," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2638–2646, Oct. 2011.

[2] S. P. Valsan and K. S. Swarup, "High-speed fault classification in power lines: Theory and FPGA-based implementation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1793–1800, May 2009.

[3] P. Rodriguez, A. V. Timbus, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Flexible active power control of distributed power generation systems during grid faults," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2583– 2592, Oct. 2007.

[4] M. F. Firuzabad, F. Aminifar, and I. Rahmati, "Reliability study of HV substations equipped with the fault current limiter," *IEEE Trans. Power Del.*, vol. 27, no. 2, pp. 610–617, Apr. 2012.

[5] A. Y. Wu and Y. Yin, "Fault-current limiter applications in medium- and high-voltage power distribution systems," *IEEE Trans. Ind. Electron.*, vol. 34, no. 1, pp. 236–242, Jan./Feb. 1998.

[6] M. Tarafdar Hagh and M. Abapour, "Non-superconducting fault current limiters," *Euro. Trans. Power Electron.*, vol. 19, no. 5, pp. 669–682, Jul. 2009.

[7] M. Tarafdar Hagh, M. Jafari, and S. B. Naderi, "Transient stability improvement using non-superconducting fault current limiter," in *Proc. IEEE 1st Power Electron. Drive Syst. Technol. Conf.*, Feb. 2010, pp. 367–370.

[8] S. H. Hosseini, M. Tarafdar Hagh, M. Jafari, S. B. Naderi, and S. Gassemzadeh, "Power quality improvement using a new structure of fault current limiter," in *Proc. IEEE ECTI_CON*,May 2010, pp. 641–645.

[9] A. Gyore, S. Semperger, L. Farkas, and I. Vajda, "Improvement of functionality and reliability by inductive HTS fault current limiter units," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 2086–2089, Jun. 2005.

[10] Y.-H. Chen, C.-Y. Lin, J.-M. Chen, and P.-T. Cheng, "An inrush mitigation technique of load transformers for the series voltage sag compensator," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2211–2221, Aug. 2010.

[11] P.-T. Cheng,W.-T. Chen, Y.-H. Chen, C.-L. Ni, and J. Lin, "A transformer inrush mitigation method for series voltage sag compensators," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1890–1899, Sep. 2007.

[12] H. Ohsaki, M. Sekino, and S. Nonaka, "Characteristics of resistive fault current limiting elements using YBCO superconducting thin film with meander-shaped metal layer," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 1818–1822, Jun. 2009.

[13] S.-H. Lim, H.-S. Choi, D.-C. Chung, Y.-H. Jeong, Y.-H. Han, T.-H. Sung, and B.-S. Han, "Fault current limiting characteristics of resistive type SFCL using a transformer," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 2055–2058, Jun. 2005.

[14] B. C. Sung, D. K. Park, J. W. Park, and T. K. Ko, "Study on a series resistive SFCL to improve power system transient stability: Modeling, simulation and experimental verification," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2412–2419, Jul. 2009.

[15] M. Abapour and M. Tarafdar Hagh, "Non-superconducting fault current limiter with controlling the magnitudes of fault currents," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 613–619, Mar. 2009.

[16] H.-S. Choi, N.-Y. Lee, Y.-H. Han, T.-H. Sung, and B.-S. Han, "The characteristic analysis between flux-coupling and flux-lock type SFCL according to variations of turn ratios," *IEEE Trans. Appl. Supercond.*, vol. 18, no. 2, pp. 737–740, Jun. 2008.

[17] M. T. Hagh, S. B. Naderi, and M. Jafari, "New resonance type fault current limiter," in *Proc. IEEE Int. Conf. PECon*, Nov./Dec. 2010, pp. 507–511.

[18] K. Arai, H. Tanaka, and M. Inaba, "Test of resonance-type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 2, pp. 650–653, Jun. 2006.

[19] H. Arai, M. Inaba, and T. Ishigohka, "Fundamental characteristics of superconducting fault current limiter using LC resonance circuit," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 2, pp. 642–645, Jun. 2006.

[20] H. G. Sarmiento, "A fault current limiter based on an LC resonant circuit: Design, scale model and prototype field tests," in *Proc. iREP Symp. Bulk Power Syst. Dyn. Control-VII, Revitalizing Oper. Rel.*, Aug. 2007, pp. 1–5.

[21] S. Henry and T. Baldwin, "Improvement of power quality by means of fault current

limitation," in *Proc. 36th Southeastern Symp. Syst. Theory*, Sep. 2004, pp. 280–284.

[22] C. Meyer and R. W. De Doncker, "LCC analysis of different resonant circuits and solid-state circuit breakers for medium-voltage grids," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1414–1420, Jul. 2006.

[23] Z. Li, M. Li, Z. Zhou, C. Zhou, D. Du, H. Liu, R. Zhan, and Z. Zhan, "Research on dynamic simulation of the resonance fault current limiter," in *Proc. Int. Conf. Power Syst. Technol.*, Oct. 2010, pp. 1–6.

[24] The MathWorks, Inc., LN: 161051 MATLAB version 7.6.0.324 (R2008a), Feb. 2008 LN: 161051.

[25] Manitoba HVDC Research Centre, LN: 684003 Licensed for University of Tabriz, LN: 684003.

[26] M. Tarafdar Hagh and M. Abapour, "DC reactor type transformer inrush current limiter," *IET Elect. Power Appl.*, vol. 1, no. 5, pp. 808–814, Sep. 2007.

[27] Globalspec, Inc., The Engineering Search Engine. [Online]. Available: http://www.globalspec.com

[28] B. Abdi, A. H. Ranjbar, G. B. Gharehpetian, and J. Milimonfared, "Reliability considerations for parallel performance of semiconductor switches in high-power switching power supplies," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2133–2139, Jun. 2009.

[29] X. He, A. Chen, H. Wu, Y. Deng, and R. Zhao, "Simple passive lossless snubber for high-power multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 3, pp. 727–735, Jun. 2006.

[30] L. Zarri, M. Mengoni, A. Tani, G. Serra, and D. Casadei, "Minimization of the power losses in IGBT multiphase inverters with carrier-based pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3695–3706, Nov. 2010.

[31] J. Bauman and M. Kazerani, "A novel capacitor-switched regenerative snubber for DC/DC boost converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 514–523, Feb. 2011.

[32] M. R. Amini and H. Farzanehfard, "Three-phase soft-switching inverter with minimum components," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2258–2264, Jun. 2011.

[33] General Atomics, Electronics Systems, High Voltage Capacitors and Power Supplies. [Online]. Available: http://www.ga-esi.com/EP

VII. AUTHORs PROFILE

B.CHITTI GOWRI received the Degree in

Electrical & Electronics Engineering completed her B.Tech from Sri Vishnu of Engineering College for Women, Affiliated to JNTU Kakinada Bhimavaram, W.G Dist, Andhra Pradesh. And currently pursuing M.Tech in Electrical Power Electronics at KITS College of Engineering, Divili, East Godavari Dist, Andhra Pradesh, Her areas of interest are Power Electronics, Power Systems and Electrical Machines.

KAKADA ARUN KUMAR working as Assistant

Professor in Kakinada Institute Of Technology And Sciences Divili , East Godavari Dist, Andhra Pradesh,. He received the Degree in Electrical & Electronics Engineering completed his B.Tech., from Pragati Engineering College Peddapuram, East Godavari, AP. Then he completed M.Tech., in Power Electronics his specialization at KITS DIVILI Kakinada, East Godavari, JNTUK, A.P, He has a teaching experience of 5 years. His area of interest is Power Systems, Power electronics, Electrical Machines & Electrical Measurements.

